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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/723,104

11/26/2003

Ketan Padalia

ALTRP196/A1103

1304

51501

7590

05/09/2008

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EXAMINER

NGO, CHUONG D

ART UNIT

PAPER NUMBER

2193

MAIL DATE

DELIVERY MODE

05/09/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/723,104	<b>Applicant(s)</b> PADALIA ET AL.	
	<b>Examiner</b> Chuong D. Ngo	<b>Art Unit</b> 2193	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 March 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 9, 10 and 12-15 is/are rejected.
- 7) ☐ Claim(s) 4-8 and 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3,9 and 10 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Tavana et al. (5,682,107) .

As per claims 1-3, Nakaya discloses in figure 1 a programmable logic device (100) including a plurality of logic array blocks (101) connected by a PLD routing architecture (see figure 2B), wherein at least one LAB includes a logic element (300, see figures 3A, and 5A) configurable to arithmetically combine a plurality of binary input signals (AB) in a plurality of stages, the LE comprising look-up table logic having K inputs (a "K-LUT") including a plurality of portions (F,J,H,J) each portion connected to a routing architecture (see figure 3A) via an input line network and having circuitry for generating binary result signals(H,C) indicative separate one a plurality of stages of the arithmetic combination of binary input signals, and providing the binary result signal to an output line network, wherein the input line network and the output line

network have input multiplexers and output multiplexers, respectively, as claimed (see figure 3A-3C).

As per claims 9 and 10, the input line network as disclosed in figures figure 3A-3C clearly has a plurality of multiplexer configurable to perform selection functions as claimed.

4. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana et al. (5,682,107) in view of Rose et al. (5,724,276).

Tavana et al. as explained above discloses the invention substantially as claimed. Tavana et al. also discloses in figure 5A a first K-LUT portion including a first sub-portion (F) and a sub-second portion (G) and a second K-LUT portion including a third sub-portion (H) and a fourth sub-portion (J). It is noted the Tavana et al does not disclose least one output multiplexer coupled to select among signals at the output of the K-LUT under the control of a carry in signal from a preceding K-LUT portion to the logic element as claimed. However, Rose et al disclosed in figure 2b additional circuit elements including an output multiplexer (F5) coupled to select among signals at the output of the K-LUT under the control of a carry in signal from a preceding K-LUT portion to the logic element. It would have been obvious to a person of ordinary skill in the art to provide Tavana et al. with additional circuit element as taught by Rose et al in order to implement additional useful function in an efficient manner (see bridging paragraph of cols. 1 and 2 in Rose et al.)

5. Claims 4-8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis, Jr. A. Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Chuong D Ngo/  
Primary Examiner, Art Unit 2193